

Atty Docket No. JCLA8534

Serial No. 10/055,499

AMENDMENTSIN THE CLAIMS**Claims 1-60. (canceled)**

61. (currently amended) A chip packaging method comprising:

providing an organic substrate with a surface;

providing a plurality of dies, wherein each die has an active surface, a backside that is opposite to the active surface, and a plurality of metal pads located on the active surface, ~~whereas the backside of each die is adhered to the surface of the organic substrate;~~

mounting the dies over the organic substrate, the backside of the dies facing the organic substrate;

forming a plurality of patterned lines over the active surface of the dies; and

performing a singularizing process to form multiple chip package structures, each having a single die or a plurality of dies.

~~allocating a first dielectric layer on top of the surface of the organic substrate and the active surface of the dies; and~~

~~allocating a first patterned wiring layer on top of the first dielectric layer, wherein the first patterned wiring layer is electrically connected to the metal pads of the dies through the first dielectric layer, extends to a region outside of an area above the active surfaces of the dies, and has a plurality of first bonding pads.~~

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62. (original) The method of claim 61, wherein the dies perform same functions.

63. (original) The method of claim 61, wherein the dies perform different functions.

64. (withdrawn) The method of claim 61, wherein the organic substrate has a plurality of inwardly protruded areas located on the surface of the organic substrate, where the backside of each die is adhered to a bottom of an inwardly protruded area.

65. (withdrawn) The method of claim 64, wherein the organic substrate comprising at least a first insulating core board and a second insulating core board formed overlapping, wherein the first insulating core board has a plurality of openings used to form inwardly protruded areas with the second insulating core board.

66. (withdrawn) The method of claim 64, wherein the openings and the organic substrate are formed together and a method of fabricating the organic substrate comprising injection molding.

67. (withdrawn) The method of claim 64, wherein the organic substrate comprising an organic layer and a heat conducting layer formed overlapping, a surface of the organic substrate is a side of the heat conducting layer that is further away from the organic layer, the organic layer has a plurality of openings that penetrates through the organic layer used to form the inwardly protruded areas, and the backside of the dies is adhered to a bottom of the inwardly protruded areas.

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68. (withdrawn) The method of claim 67, wherein the openings and the organic substrate are formed together and a method of fabricating the organic substrate comprising injection molding.

69. (withdrawn) The method of claim 67, wherein the heat conducting layer comprising a metal.

70. (currently amended) The method of claim 61, further comprising forming a filling layer over the organic substrate and surrounding the peripheral region of the dies after mounting the dies onto the organic substrate, wherein a top surface of the filling layer is planar to the active surface of the dies and the patterned lines are formed over the filling layer. ~~wherein after adhering the dies and before allocating the first dielectric layer, further comprising allocating a filling layer on top of the surface of the organic substrate and surrounding the peripheral of the dies, and a top surface of the filling layer is planar to the active surface of the dies.~~

71. (original) The method of claim 70, wherein a material of the filling layer is selected from a group consisting of epoxy and polymer.

72. (currently amended) The method of claim 61, further comprising forming a dielectric layer over the active surface of the dies after mounting the dies over the organic substrate and before forming the patterned lines over the active surface of the dies. ~~wherein after allocating the first dielectric layer and before allocating the first patterned wiring layer, further comprising patterning the first dielectric layer to form a plurality of first thru holes that penetrates through~~

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the first dielectric layer, and the first patterned conductive is electrically connected to the metal pads of the dies by the first thru holes.

73. (currently amended) The method of claim 72, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material. ~~when allocating the first patterned wiring layer on the first dielectric layer, further includes allocating a plurality of first vias by filling part of a conductive material of the first patterned conductive layer into the first thru holes to electrically connect the first patterned wiring layer and the metal pads of the dies by the first vias.~~

74. (currently amended) The method of claim 61-72, further comprising forming a dielectric layer over the patterned lines after forming the patterned lines over the active surface of the dies. ~~wherein when allocating the first patterned wiring layer on top of the first dielectric layer, further comprising filling the first thru holes with a conductive material to form a plurality of first vias, by which the first patterned wiring layer and the metal pads are electrically connected.~~

75. (currently amended) The method of claim 74-61, wherein a material of the first dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.

76. (currently amended) The method of claim 61, wherein the step of forming the patterned lines over the active surface of the dies is provided by a technology comprising

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electroplating. ~~the method of allocating the first patterned wiring layer on top of the first dielectric layer is selected from a group consisting of sputtering, electroplating, and electro-less plating.~~

77. (currently amended) The method of claim 61, wherein the step of forming the patterned lines over the active surface of the dies is provided by a technology comprising sputtering and electroplating. ~~further comprising allocating a patterned passivation layer on top of the first dielectric layer and the first patterned wiring layer and exposing the first bonding pads.~~

78. (currently amended) The method of claim 61, further comprising depositing a plurality of bonding points on a plurality of bonding pads of the patterned lines after forming the patterned lines over the active surface of the dies. ~~further comprising allocating a bonding point on the first bonding pads.~~

79. (currently amended) The method of claim 78, wherein the bonding points comprise solder balls. ~~wherein the bonding points are selected from a group consisting of solder balls, bumps, and pins.~~

80. (currently amended) The method of claim 61-78, wherein a material of the organic substrate comprises plastic. ~~further comprising singularizing the chip package structure after allocating the bonding point on the bonding pads.~~

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81. (currently amended) The method of claim 61-80, wherein a material of the organic substrate comprises thermosetting plastic. ~~a singularization of the chip package structure is performed on a single die.~~

82. (withdrawn) The method of claim 80, wherein a singularization of the chip package structure is performed on a plurality of dies.

83. (currently amended) The method of claim 61, wherein the step of forming the patterned lines over the active surface of the dies comprises forming a single patterned wiring layer. ~~further comprising:~~

~~—————(a) allocating a second dielectric layer on top of the first dielectric layer and the first patterned wiring layer; and~~

~~—————(b) allocating a second patterned wiring layer on top the second dielectric layer, wherein the second patterned wiring layer is electrically connected to the first patterned wiring layer through the second dielectric layer, and the second patterned wiring layer extends to a region outside the active surface of the die and has a plurality of second bonding pads.~~

84. (currently amended) The method of claim 61-83, wherein the step of forming the patterned lines over the active surface of the dies comprises forming a plurality of patterned wiring layers and at least a dielectric layer, the dielectric layer formed between the patterned wiring layers. ~~wherein after allocating the second dielectric layer and before allocating the second patterned wiring layer, further comprising patterning the second dielectric layer to form a~~

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plurality of second thru holes, which corresponds to the first thru holes and penetrates the second dielectric layer, to electrically connect to the first patterned wiring layer.

85. (currently amended) The method of claim 84, wherein a material of the dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material. ~~wherein when allocating the second patterned wiring layer on top of the second dielectric layer, further comprising filling the second thru holes with part of a conductive material of the second patterned wiring layer to form a plurality of second vias, by which the second patterned wiring layer is electrically connected to the first patterned wiring layer.~~

86. (currently amended) The method of claim 61-84, wherein a material of the organic substrate comprises polymer resin. ~~wherein before allocating the second patterned wiring layer on top of the second dielectric layer, further comprising filling the second thru holes with a conductive material to form a plurality of second vias, by which the second patterned wiring layer is electrically connected to the first patterned wiring layer.~~

87. (currently amended) The method of claim 61-83, wherein a material of the organic substrate comprises epoxy resin. ~~wherein a material of the second dielectric layer is selected from a group consisting of polyimide, benzocyclobutene, porous dielectric material, and stress buffer material.~~

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88. (currently amended) The method of claim 83, wherein a material of the organic substrate comprises imide resin. ~~wherein the method of allocating the second patterned wiring layer on the second dielectric layer is selected from a group consisting of sputtering, electroplating, and electro-less plating.~~

89. (currently amended) The method of claim 83, wherein the patterned lines comprises copper. ~~further comprising allocating a patterned passivation layer on top of the second dielectric layer and the second patterned wiring layer and exposing the second bonding pads.~~

Claims 90-175. (canceled)